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09/264,085	03/08/1999	YOUSSEF ABDELILAH	RA9-98-074	2597

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EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	19

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

	Application No.	Applicant(s)
Office Action Summary	09/264,085	ABDELILAH ET AL.
	Examiner	**Art Unit**
	Pankaj Kumar	2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If tha period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from tha mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statuta, causa tha application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Offica later than three months after the mailing date of this communication, even if timely filed, may reduca any earnad patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/11/2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-14,16-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,6-11 and 28-30* is/are allowed.

6)☒ Claim(s) *12,17,19,20,22,24,25 and 27* is/are rejected.

7)☒ Claim(s) *13,14,16,18,21 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 24 recites the limitation "claim 24". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 12, 17, 19, 20, 22, 24, 25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by McDonough USPN 5,778,024

1. Regarding claim 12, McDonough teaches a method for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock (inherent), comprising the steps of:

2. sampling the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock (McDonough fig. 2: 110);

3. <u>generating first and second integers in response to a sampling index signal using a time converter</u> (McDonough paragraph 49: "The resulting energy estimates are sampled every 80 ms by (400:1) decimation elements 641, 651 and 659."; 621) (decimator is the time converter; x is the sampling index signal in fig. 6 with 1/400x; first and second integers are the serial outputs of any one of 621, 641, 651, 659);

4. interpolating (McDonough fig. 5C: 608 is interpolating and fig. 5C is element 550 which is shown in fig. 5A which is shown in fig. 5A to be after fig. 6's element 490) the digital samples <u>in response to the first integer</u> to produce first and second estimates for each of the digital samples (inherent if I and Q samples existed) using a polyphase interpolator (McDonough element 608 works on multiple phases of the signal and thus is polyphase);

5. interpolating (McDonough fig. 5A: 46, 406, 416; fig. 5A, 5B: 426, 592) the first and second estimates (McDonough fig. 5A: two serial outputs of 550) <u>in response to the second integer</u> (McDonough fig. 5A, 6: the second integer output in series from any one of 621, 641, 651, 659 goes into fig. 5A: 46; fig. 5A, 5B: 426, 592 via other components) to produce interpolated digital samples having a second local sample rate (McDonough fig. 5C which is part of fig. 5A has 3x interpolation while 460 in fig. 5A has 2:5 interpolation) that is synchronized with the network clock (McDonough fig. 1: external timing) using a linear interpolator (McDonough fig. 5A: 406, 416 are linear filters which when combined with the interpolation produce linear interpolation);

6. equalizing (McDonough fig. 4: 338, 348) the interpolated digital samples to produce equalized digital samples; and decoding the equalized digital samples to generate detected symbols therefrom (McDonough fig. 4: 346, 350, fig 5C: 292, fig. 5A, fig. 6).

7. Regarding claim 17, a method as recited in Claim 12, further comprising the step of identifying a signaling alphabet (McDonough "code excited linear prediction" – CELP, the input into the decoder is the signaling alphabet that is identified) for use in the decoding step to generate the detected symbols (McDonough output of decoder).

8. Regarding claim 19, a method as recited in Claim 12, wherein the detected symbols are pulse code modulation (PCM) codewords (inherent for modulated digital signals to be PCM).

9. McDonough shows figures and logic diagrams that may be coded. Claims 20, 22, 24, 25, 27 are rejected over McDonough.

10. As per claim 20, (Twice Amended) A computer program product for demodulating, in a receiver, n data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising: a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising: first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock; second logic configured to generate first and second integers in response to a sampling index signal using a time converter; third logic configured to

interpolate the digital samples in response to the first integer to produce first and second estimates for each of the digital samples, the third logic configured to interpolate comprising: fourth logic configured to use a polyphase interpolator to produce the first and second estimates; fifth logic configured to interpolate the first and second estimates in response to the second integer to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock, the second logic configured to interpolate comprising: sixth logic configured to use a linear interpolator to produce the interpolated digital samples; seventh logic configured to equalize the interpolated digital samples to produce equalized digital samples; and eighth logic configured to decode the equalized digital samples to generate detected symbols therefrom (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

11. As per claim 22, (Amended) A computer program product as recited in Claim 20, further comprising: ninth logic configured to maintain the synchronization between the second local sampling rate and the network clock via the sampling index signal (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

12. As per claim 24, (Amended) A computer program product as recited in Claim 24, wherein the receiver further includes an echo canceller coupling a transmitter to the receiver, further comprising: ninth logic configured to receive at an input of the echo canceller transmit symbols from the transmitter that have a third local sample rate that is synchronized with the local clock; and tenth logic configured to generate at an output of the echo canceller echo

cancellation samples at the first local sample rate in synchronization with the local clock (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

13. As per claim 25, (Amended) A computer program product as recited in Claim 20 further comprising' ninth logic configured to identify a signaling alphabet, the eighth logic configured to decode being responsive to the logic configured to identify (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

14. As per claim 27, a computer program as recited in claim 20, wherein the detected symbols are pulse code modulation (PCM) codewords (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

Allowable Subject Matter

15. Claims 1, 2, 3, 6-11, 28, 29, 30 are allowed.

16. Claims 13, 14, 16, 18, 21 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:
The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with the following underlined portions which are bolded and italicized:

18. As per claim 1, what McDonough teaches is a receiver for demodulating a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

19. a two-stage interpolator (McDonough figs. 5A, 5B, 5C: 426, 592, 460, 550, 608), responsive to digital samples of the data signal, that generates interpolated digital samples in response thereto, the digital samples having a first local sample rate that is synchronized with a local clock and the interpolated digital samples having a second local sample rate that is synchronized with the network clock (inherent for there to be two different clocks since there are multiple interpolations and we want to save power – if interpolations at two rates, we do not want both clocks to run at the fastest rate required for the fastest interpolation), wherein the two-stage interpolator comprises:

20. <u>a time converter responsive to a sampling index signal, that generates first and second integers in response thereto;</u>

21. a polyphase interpolator, responsive to the digital samples of the data signal <u>and the first integer</u>, that generates first and second estimates for each of the digital samples of the data signal; and

22. a linear interpolator, responsive to the first and second estimates <u>and the second integer</u>, that generates the interpolated digital samples;

23. an <u>***adaptive fractionally spaced decision feedback equalizer***</u> (not in McDonough), responsive to the interpolated digital samples, that generates equalized digital samples at the network sampling rate in synchronization with the network clock; and a slicer, responsive to the

equalized digital samples, that generates detected symbols therefrom corresponding to data from the data signal (remainder discussed in other claims especially claim 12).

24. Claims 2, 3, 6-11 are allowable since they depend on claim 1.

25. As per claim 28, what Orban shows is a receiver (Orban fig. 2) for demodulating a data signal transmitted from a digital source (Orban col. 2 lines 26-27 "digital medium") at a network sampling rate that is synchronized with a network clock (inherent since data is being sampled), comprising:

26. a two-stage interpolator (Orban fig. 2: 200,201), responsive to digital samples of the data signal, that generates interpolated digital samples in response thereto, the digital samples having a first local sample rate that is synchronized with a local clock and the interpolated digital samples having a second local sample rate that is synchronized with the network clock (inherent for there to be two different clocks since there are multiple interpolations and we want to save power). What Orban does not show is an adaptive fractionally spaced decision feedback equalizer, responsive to the interpolated digital samples, that generates equalized digital samples at the network sampling rate in synchronization with the network clock; and a slicer (Orban fig. 2: 400, 401), responsive to the equalized digital samples, that generates detected symbols therefrom corresponding to data from the data signal. What Serfaty shows is a decision feedback equalizer (Serfaty fig. 4: 39) after interpolation (Serfaty fig. 4: 36) within the same field of endeavor. What Orban shows is a slicer (Orban fig. 2: 400, 401) that generates detected symbols corresponding to data from the data signal; however, since there is no DFE in Orban, this slicer

is not responsive to equalized digital samples. It would have been obvious to one skilled in the art at the time of the invention to modify Orban to include a DFE of Serfaty after the interpolations since they are both in the same field of endeavor and doing so would result is a better performing system; means for identifying a signaling alphabet used by the slicer to generate the detected symbols (Orban fig. 1: 60 shows a clipper – one letter in the alphabet); means for establishing a plurality of alphabetic thresholds (Yoshida USPN 4792964 "The output of multiplier 3 is coupled to a decision circuit 4 which converts it to a signal having discrete amplitude levels by comparison with multiple decision thresholds."); ***means for computing an average value for the equalized digital samples corresponding to a particular alphabet threshold (not in the cited references)***.

27. As per claim 29, Orban shows a method for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock (inherent), comprising the steps of:

28. sampling the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock (Orban sampling for fig. 2: 200);

29. interpolating the digital samples to produce first and second estimates for each of the digital samples (inherent if I and Q samples existed in Orban);

30. interpolating the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock (Orban sampling for fig. 2: 201)

31. What Orban does not show is equalization. What Serfaty shows (as discussed above) is equalizing the interpolated digital samples to produce equalized digital samples; and decoding the equalized digital samples to generate detected symbols therefrom.

32. identifying a signaling alphabet … comprising the steps of establishing a plurality of alphabetic thresholds (Yoshida USPN 4792964 "The output of multiplier 3 is coupled to a decision circuit 4 which converts it to a signal having discrete amplitude levels by comparison with multiple decision thresholds."); ***computing an average value for the equalized digital samples corresponding to a particular alphabet threshold (not in the cited references)*** …

As per claim 30, (Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising: a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising: first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock; second logic configured to interpolate the digital samples to produce first and second estimates for each of the digital samples; third logic configured to interpolate the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock; fourth logic configured to equalize the interpolated digital samples to produce equalized digital samples; fifth logic configured to decode the equalized digital samples to generate detected symbols therefrom; sixth logic configured to identify a signaling alphabet, the fifth logic configured to decode being responsive to the logic configured to identify, the sixth logic configured to identify comprising: seventh logic configured to

establish a plurality of alphabet thresholds corresponding to valid data symbols; eighth logic configured to ***compute an average value for the equalized digital samples corresponding to a particular alphabet threshold*** (not in McDonough); and ninth logic configured to update the particular alphabet threshold with the average value (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

33. Regarding claim 13. A method as recited in Claim 12, wherein ***the equalizing step comprises the step of using an adaptive fractionally spaced decision feedback equalizer that has a tap spacing given by pTlq where T is a modulation interval associated with the network sampling rate and p and q are integers to produce the equalized digital samples*** (not in McDonough).

34. Regarding claim 14, McDonough teaches a method as recited in Claim 12, further comprising the step of: ***maintaining the synchronization between the second local sample rate and the network clock via ~~a~~ the sampling index signal*** (not in McDonough).

35. Regarding claim 16, a method as recited in Claim 12, further comprising the steps of: coupling a transmitter to the receiver with an echo canceller (McDonough fig. 4: 338, 348 equalize to cancel echo); ***receiving at an input of the echo canceller transmit symbols from the transmitter that have a third local sample rate that is synchronized with the local clock*** (not in McDonough); and generating at an output of the echo canceller echo cancellation samples at the first local sample rate in synchronization with the local clock (discussed above).

36. As per claim 18, a method as recited in claim 17, wherein the identifying step comprises the steps of: establishing a plurality of alphabet thresholds corresponding to valid data symbols (McDonough fig. 4: CELP is a predictor which establishes the thresholds corresponding to the valid inputs); ***computing an average value for the equalized digital samples corresponding to a particular alphabet threshold*** (not in McDonough); and updating the particular alphabet threshold (McDonough fig. 4: purpose of prediction) with the average value.

37. As per claim 21, (Amended) A computer program product as recited in Claim 20, wherein the seventh logic configured to equalize comprises: ninth logic configured to use ***an adaptively fractionally spaced decision feedback equalizer that has tap spacing given by pTIq where T is a modulation interval associated with the network sampling rate and p and q are integers to produce the equalized digital samples*** (not in McDonough).

38. As per claim 26. (Amended) A computer program product as recited in Claim 25, wherein the ninth logic configured to identify comprises: tenth logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols; eleventh logic configured to ***compute an average value for the equalized digital samples corresponding to a particular alphabet threshold*** (not in McDonough); and twelfth logic configured to update the particular alphabet threshold with the average value (McDonough shows figures and logic diagrams that may be coded. Remainder discussed above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

PK
May 22, 2003

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 5/27/03